ABSTRACT OF THE DISCLOSURE

An input buffer circuit without a drop of a capability of a circuit and a limitation of a connection type with a circuit of a former stage is obtained. The output signal (OUTB) is inputted to a first low pass filter circuit, and the first low pass filter circuit integrates the output signal (OUTB). A result of the integration is stored as a voltage value (V2a) in the capacitor (4s). In the same manner, an output signal (OUT) is inputted to a second low pass filter circuit, and the second low pass filter circuit integrates the output signal (OUT). A result of the integration is stored as a voltage value (V2b) in a capacitor (4t). A differential amplifier circuit (5) generates appropriate voltages (V3a and V3b) according to a design specification of the transistors (1x and 1y) by amplifying the voltage values (V2a and V2b) and outputs them. The voltages (V3a and V3b) are impressed on respective back gates of the transistors (1x and 1y), respectively.